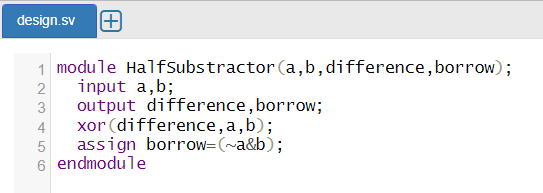
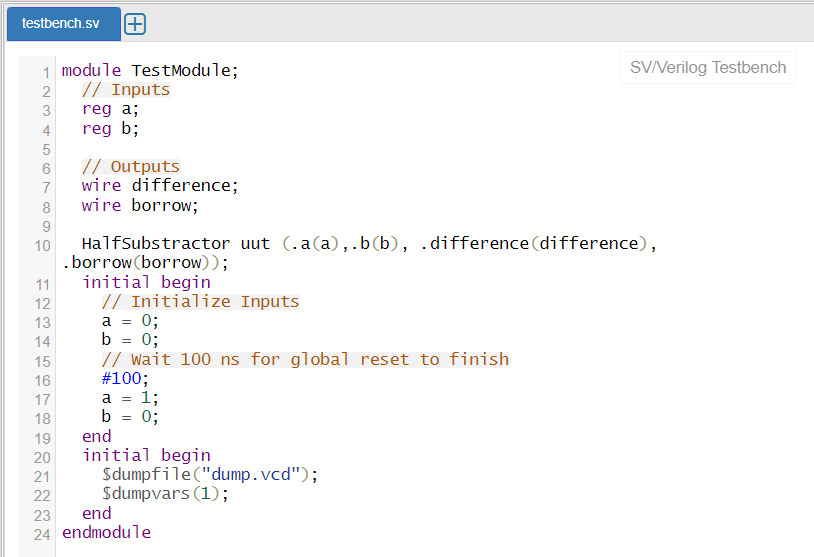
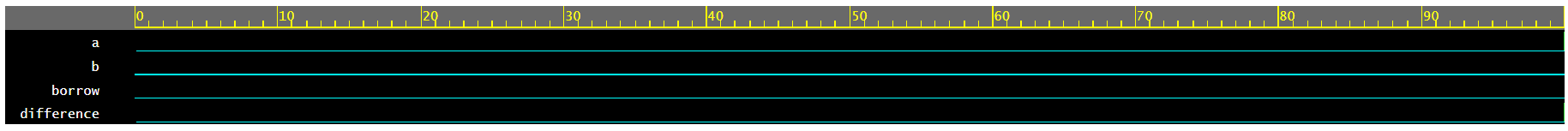
**LAB 5: Design Half Subtractor, Full Subtractor Using Half Subtractors**

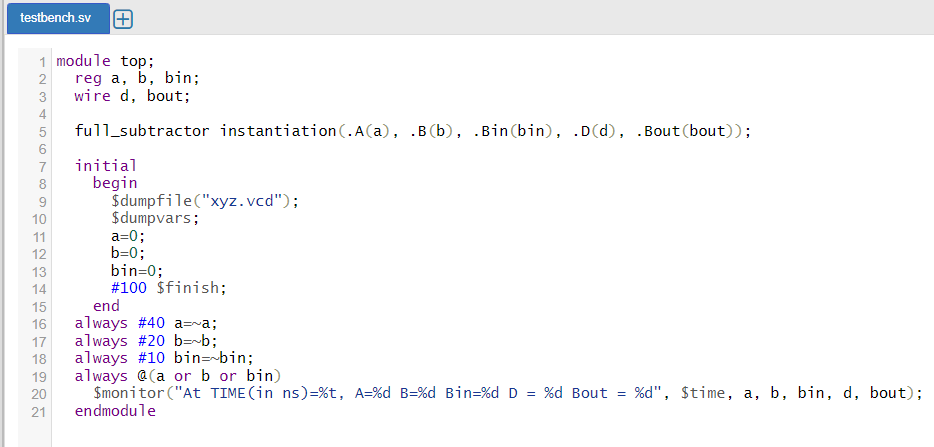
**Question 1: Write a Verilog code to design a Half subtractor and test it using the Waveform**

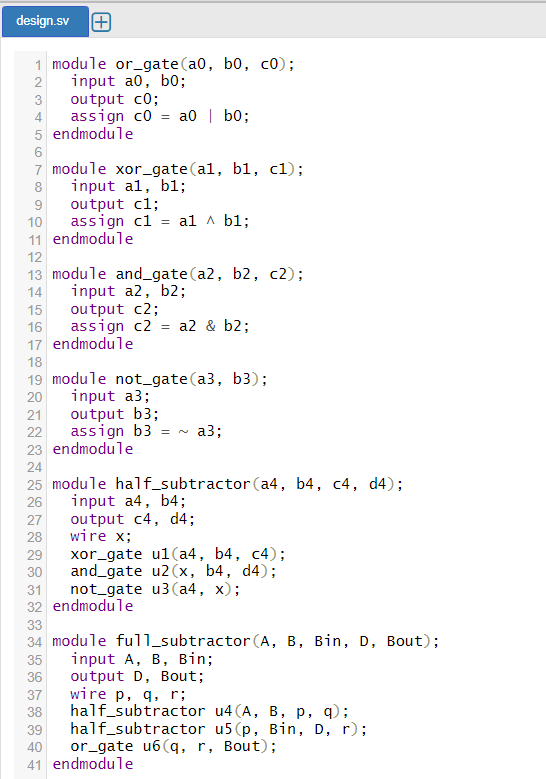
****

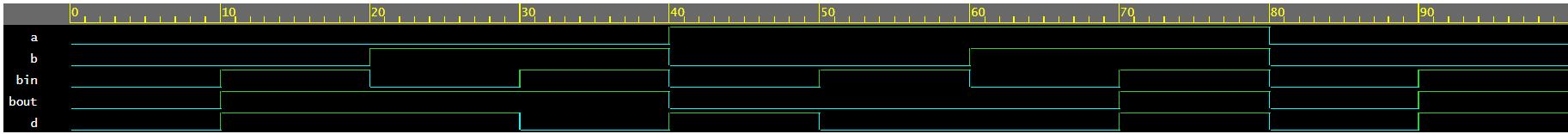
****

****

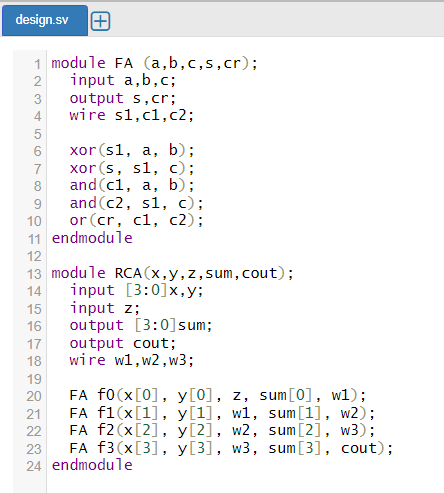
**Question 2: Write a Verilog code to design a Full subtractor using Half subtractors and test it using the Waveform.**

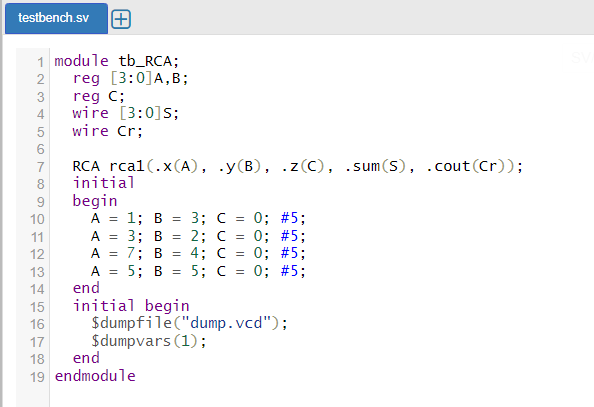
****

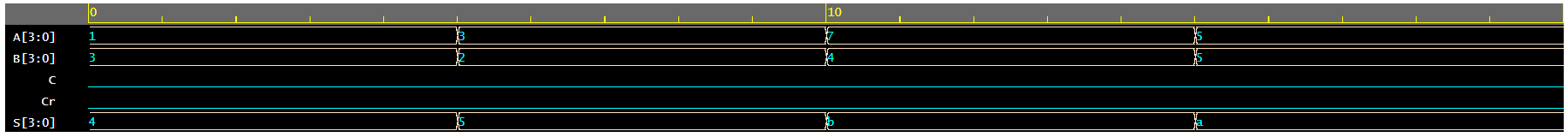
****

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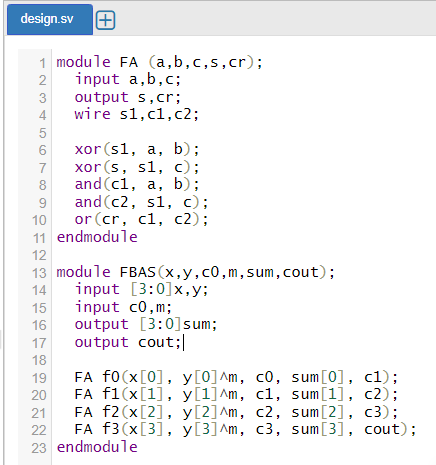
**Question 3: Write the Verilog code (either structural or behavioural) for a 4-bit ripple carry adder. The block diagram of a 4-bit ripple carry adder has been given in Figure 1 for your reference.**

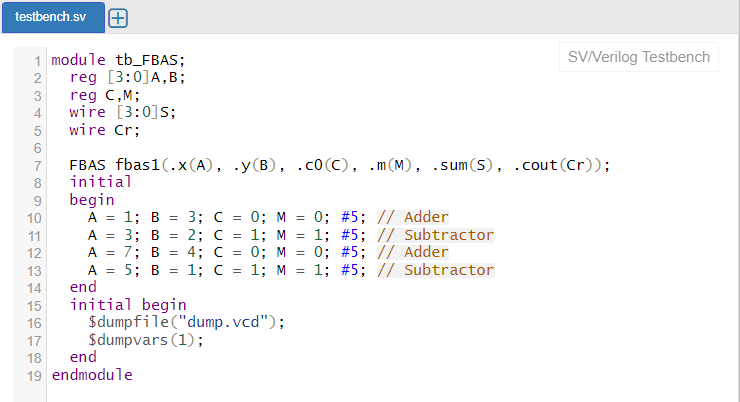
****

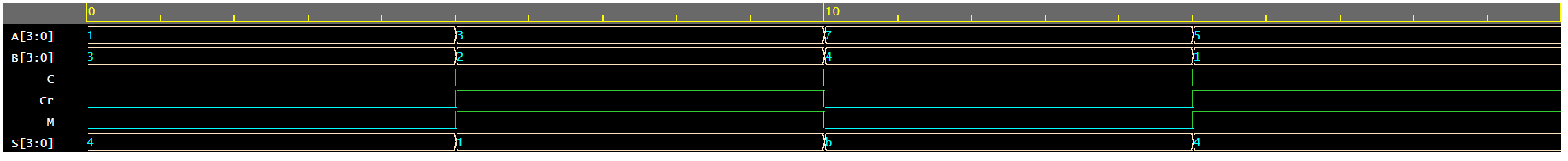
****

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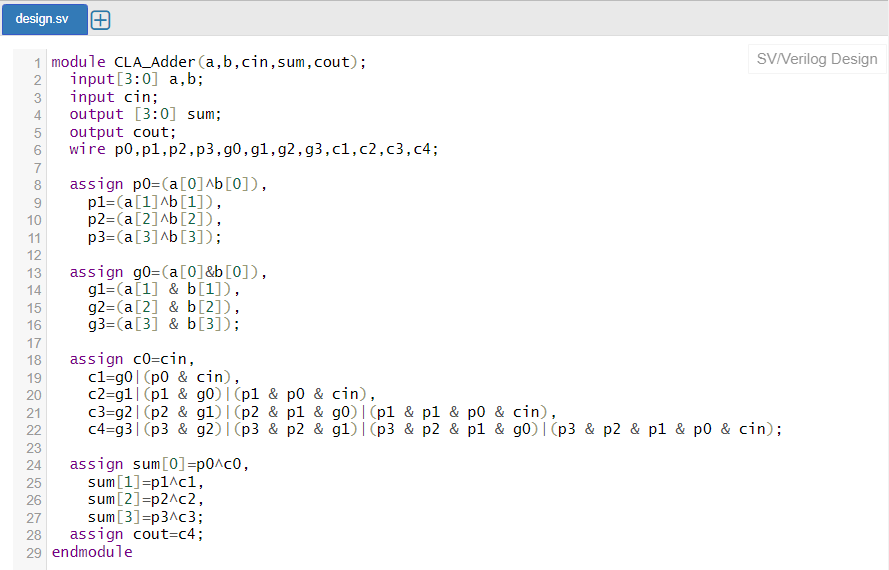
**Question 4: Write the Verilog code to construct a 4-bit adder-subtractor using. The logic diagram of a 4-bit adder-subtractor using a ripple carry adder has been given in Figure 2 for your reference.**

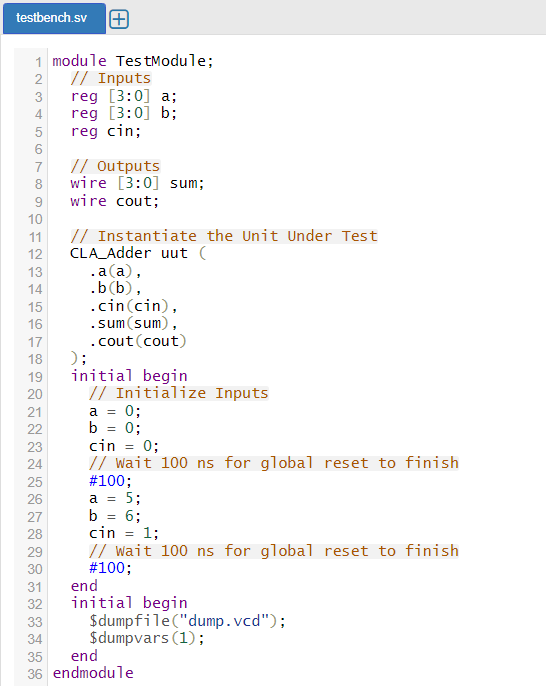
****

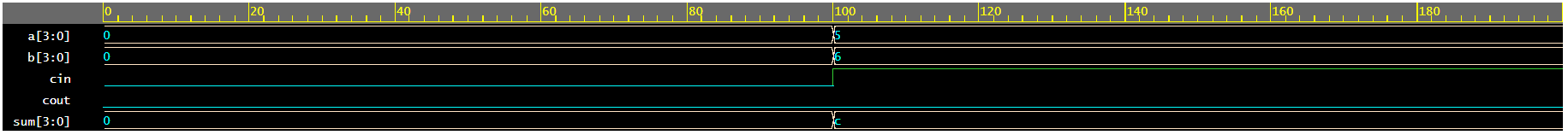
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**Question 5: Write the Verilog code for a 4-bit carry look-ahead adder (CLA). The block diagram of the same has been given in Figure 3.**

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